IDEC Chip Design Contest

7.5-GHz Low LO pumping Cryo-CMOS Parametric Amplifier for Quantum Computing

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Abstract

- This paper presents the design of a cryo-CMOS parametric amplifier suitable for operation at 4K and mK temperatures within the readout chain of quantum computers. The measured gain is 0dB with 20dBm LO power at 300K, and 15.2dB with 0dBm LO power at 4K.

Introduction

- CMOS parametric amplifiers (CPA) offer a scalable solution for qubit readout at both 4 K and millikelvin temperatures [1].
- The benefits of CPA are achievable only with noise performance comparable to HEMT LNAs.

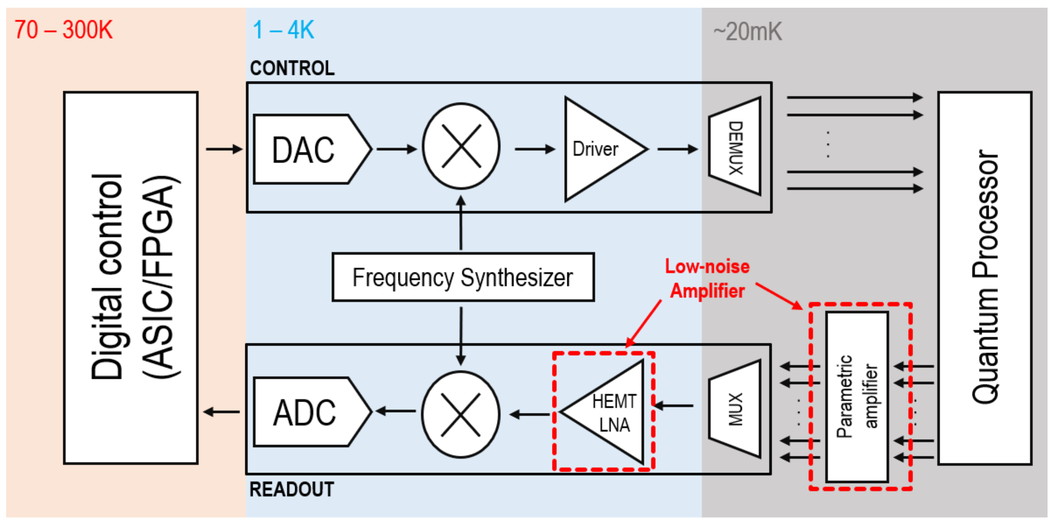

Fig. 1. RF reflectometry qubit readout block diagram

	JPA [2]	CPA [3]	HEMT LNA [4]
Temperature	mK	mK / 4K	4K
P1dB	~ –115 dBm	~ – 57 dBm	- 53 dBm
DC power	X	X	~10mA

→ In this work, a CMOS-based single-balanced mixer-type parametric amplifier combined with a diplexer is proposed for low-power and compact-area implementation.

Amplifier Design

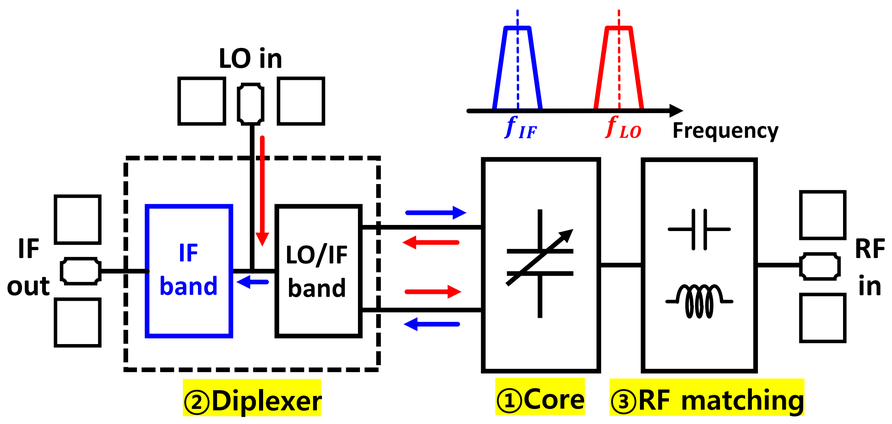

Fig. 2. Proposed parametric amplifier block diagram

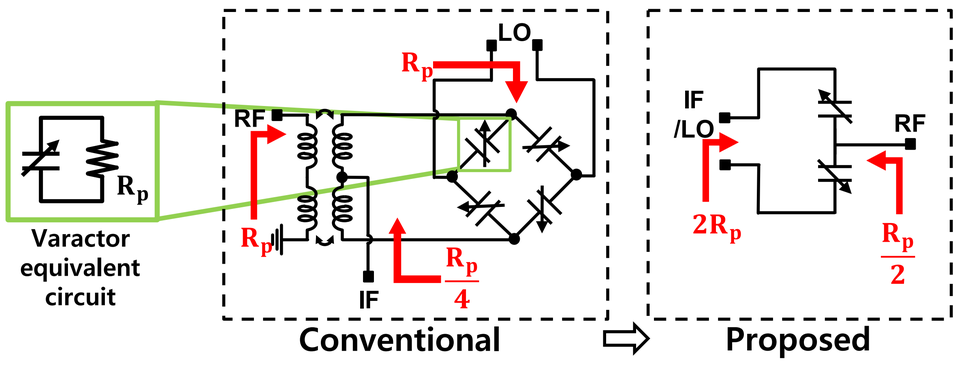

Fig. 3. Core structure of conventional and proposed parametric amplifier

➢ Core Structure

- $R_{p,LO}$ and $R_{p,RF/IF}$ X2↑ → gain and noise performance at reduced LO power.

➢ Diplexer Structure for LO/IF Matching

- Forming a LPF at f_{IF} → higher gain by G_{IF}↓
- Acting as an LO short → LO-IF isolation even in a single-balanced structure.

Fig. 4. Operation of Diplexer at IF and RF frequency

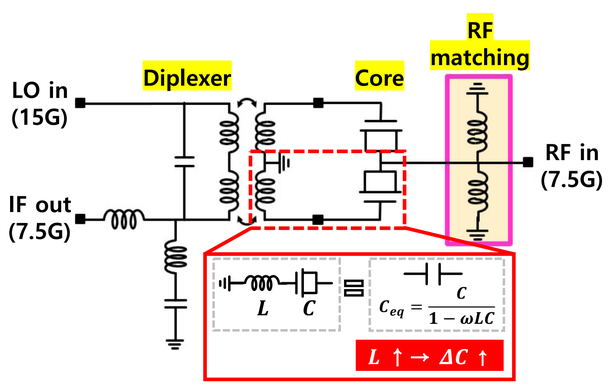

Fig. 5. Full schematic of the CPA

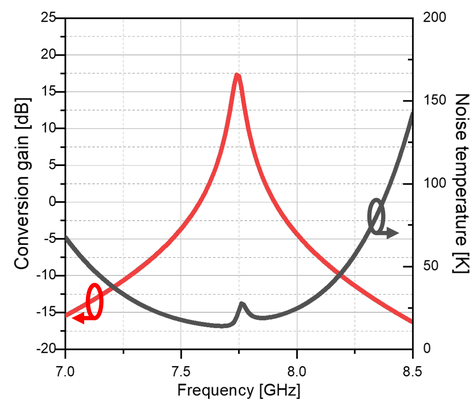

Fig. 6. Simulated conversion gain and noise temperature at 4K

➢ RF Matching Network

- Increasing ΔC by series inductor in the diplexer → higher gain
- The parallel inductors → lowering G_{RF} for RF matching

➢ Simulation Results

- Simulated with P_{LO} of -10dBm at 4K → conversion gain of 17.3dB & min. noise temperature of 14.2K.

Measurement

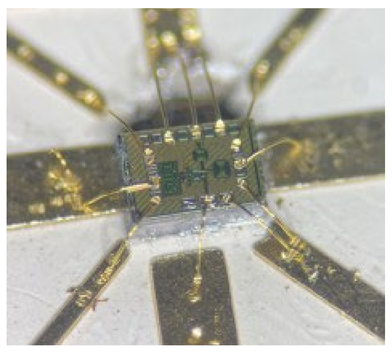

Fig. 7. A photograph of die chip

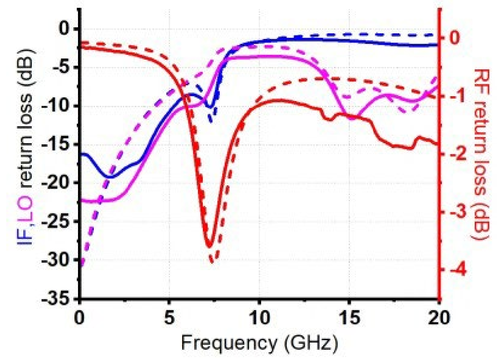

Fig. 8. Return-loss at 300K

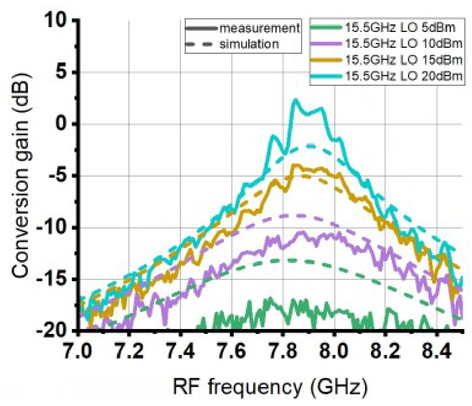

Fig. 9. Conversion-gain at 300K

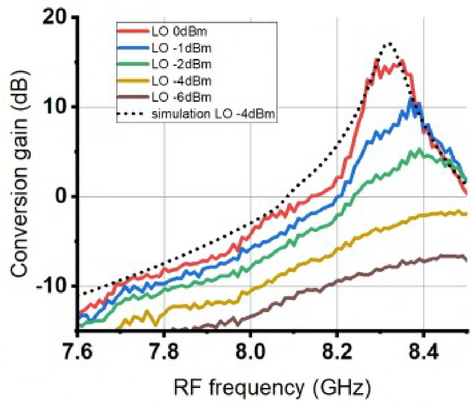

Fig. 10. Conversion-gain at 4K

- Chip size : 0.66 mm × 0.79 mm = 0.52 mm^2
- Return-loss at 300K: RF and IF ports are matched at 7.5 GHz, and the LO port is matched at 15 GHz.
- Conversion-gain at 300K: 2.5 dB with a 15.5 GHz LO at 20 dBm.
- Conversion-gain at 4K: 15.2 dB with a 16.4 GHz LO at 0 dBm.

Reference [1] M. Mehrpoo et al., *IEEE L-SSC*, 2019. [2] J. Aumentado, *IMS*, 2022. [3] G. Baek et al., *IEEE Symp. VLSI Technol. Circuits*, 2022. [4] LNF-LNC4_8C: 4-8GHz Cryogenic LNA , *Low Noise Factory*, 2018

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